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ATTORNEY'S DOCKET NO: S1022.80363US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Patentee:	Geoff BARRETT		
Serial No:	09/477,790	Patent No.	6,816,821
Filed:	December 31, 1999	Issued:	November 9, 2004
For:	POST IMAGE TECHNIQUES		
Examiner:	Herng Der Day		
Art Unit:	2123	Confirmation No.	9742

ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate
AUG 15 2005
of Correction

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

[X] Request for Certificate of Correction
[X] Copies of: Page 3 from 12/08/03 Amend and Col. 5 of U.S. 6,816,821.
[X] PTO Form SB/44
[X] Return Post Card

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617)720-3500, Boston, Massachusetts.

No check is enclosed. If it is determined that a fee is necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on August 3, 2005.

Attorney Docket No.: S1022.80363US00
XNDD

Respectfully submitted,

Geoff Barrett, Patentee

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE
OF CORRECTION UNDER 37 C.F.R. §1.322

Sir/Madam:

Patentee respectfully requests the correction of an error found in the above-captioned patent. Specifically, an amendment to the text was not updated in issued U.S. Patent No. 6,816,821.

In column 5, lines 32-40 of issued U.S. Patent No. 6,816,821 currently read:

> A processor 400 further includes a forming device 440 which receives the state variables of the real/reverse models from the third store 300 and also receives the transition functions of the reverse machine from the fourth store 500 and acts to substitute the state variables of the reverse machine with the transition functions of the reverse machine to provide a new set of states which represent the pre-image of the reverse system thus the post-image of the **second** system. This data is stored in fifth store 600. (Emphasis added)

However, in an amendment filed on December 8, 2003 the word "second" was replaced with the word "real." This paragraph found in column 5, lines 32-40, as amended should read as shown below.

> A processor 400 further includes a forming device 440 which receives the state variables of the real/reverse models from the third store 300 and also receives the transition functions of the reverse machine from the fourth store 500 and acts to substitute the state variables of the reverse machine with the transition functions

of the reverse machine to provide a new set of states which represent the pre-image of the reverse system thus the post-image of the **real** system. This data is stored in fifth store 600. (Emphasis added)

In support of this Request Patentee submits herewith a highlighted copy of page 3 of the amendment filed on December 8, 2003 and column 5 of U.S. 6,816,821.

Patentee requests that a Certificate of Correction be granted in U.S. Letters Patent No. 6,816,821 as specified herein and on the attached Certificate of Correction form SB/44.

The correction requested does not involve change in the patent that constitutes new matter or would require reexamination. Therefore, it is respectfully requested that the corrections be made and that a Certificate of Correction be issued.

Patentee respectfully submits that, since the error for which a Certificate of Correction is sought was the result of Patent Office mistake, no fee is due. However, if the Examiner deems a fee necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825.

Should any questions arise concerning the foregoing, please contact the undersigned at the telephone number listed below.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on August 3, 2005.

Gail Driscoll

Attorney Docket No.: S1022.80363US00US00
XNDD

Respectfully submitted,

Geoff Barrett, Patentee

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system. Beginning with the transitions of the reverse system being T', the transition functions of the original system are used to constrain them. Thus, for each state s and transition t, there is a constraint S=t[S:=S']. Call the set of constraints C. For each constraint, the parameterization E over the variables S', is calculated and this is substituted in the transition functions and the remaining constraints.

The parameterization is an idempotent parameterization i.e. a parameterization which after being affected, leaves the relationship entirely unaltered.

Referring to FIG. **2**, a first store (memory) **100** stores bits representative of transition functions of a system. A second store **200** stores bits representative of estimated transition function of a reverse model of said system, the estimate being derived from knowledge of the next-state variables of the reverse system, which of course correspond to the previous state variables of the original system. A third store **300** stores bits representative of the set of state variables of the system, which necessarily is also the set of state variables of the reverse model.

A processor **400** has a logical transforming device **410** which receives the transition functions of the real machine from the first store **100** and transforms the transition functions into constraints on the reverse model. The processor further has a parameterization processing device **420** for calculating for each constraint the parameterization over the variables of the reverse machine which are then applied to the estimated transition functions of the reverse machine in applying means **430**. The applying means **430** provides an output to a fourth store **500** which stores the actual transition functions of the reverse model.

A processor **400** further includes a forming device **440** which receives the state variables of the real/reverse models from the third store **300** and also receives the transition functions of the reverse machine from the fourth store **500** and acts to substitute the state variables of the reverse machine with the transition functions of the reverse machine to provide a new set of states which represent the pre-image of the reverse system thus the post-image of the second system. This data is stored in fifth store **600**.

Referring to FIG. **3**, the method of the invention, as described above, involves forming a model of the reverse machine and then applying as inputs to the model of the reverse machine, outputs of the real machine so as to determine what inputs in the real machine could give rise to those outputs. It is therefore necessary to provide an accurate model of the reverse machine and this part of the inventive method is shown in FIG. **3**.

Referring to FIG. **3**, a complete description of the real machine **1000** is accessed and processed to extract the state transitions **1002** using a processing engine **1001**. A second processing engine **1003** also accesses the description **1000** to provide the transition functions **1004** of the real machine. A further processing stage **1005** reverses the transitions of the real machine to provide an output **1006** of reverse transitions. The transition functions in box **1004** are processed **1007** to as to transform the transition functions of the real machine into constraints and a parameterization of the constraints is applied in stage **1008** to each and all of the reverse transitions to thereby form the model of the reverse machine **1010**. As reported above, by applying the outputs of the real machine as inputs to the model of the reverse machine, the inputs to the real machine can be discovered.

The described method and device has a large number of applications such as deriving properties of a control system using a model of the system or deriving properties of a hardware system using a model of the system. The described novel technique may specifically be used for testing electronic circuits, testing logic circuits, including microprocessors. In general, the described method and device can be used for testing any mechanistic system in which states occur and transitions between the states occur on a clocked or a time-dependent basis.

The above description is of preferred and exemplary embodiment(s) of the present invention only and is to enable a full understanding of the invention while not intending to limit the invention can be ascertained from the following claims.

What is claimed is:

1. A method of synthesizing a reverse model of a finite state machine, the method comprising:

transforming a transition function of a state machine model of said finite state machine into a constraint on the reverse model, wherein the reverse model is a reverse model of the state machine model; and

applying a parameterization of said constraint to all transitions of the reverse model.

2. The method as claimed in claim **1** wherein said finite state machine includes a logic circuits.

3. The method as claimed in claim **1** wherein said finite state machine includes a microprocessor.

4. A method of calculating a post-image in a finite state machine, the method comprising:

forming a reverse model of said finite state machine, wherein the reverse model is a reverse model of a state machine model of the finite state machine; and

calculating a pre-image in said reverse model, wherein the pre-image in said reverse model is equivalent to the post-image in said finite state machine.

5. The method as claimed in claim **4** wherein said finite state machine includes a logic circuits.

6. The method as claimed in claim **4** wherein said finite state machine includes a microprocessor.

7. The method of claim **4** further comprising identifying from a characterization of a model of said finite state machine, transitions of said finite state machine and reversing said transitions to form potential transitions of a reverse model.

8. The method of claim **4** and further comprising extracting from a characterization of a model of said finite state machine, transition functions of said finite state machine.

9. A device for synthesizing a reverse model of a finite state machine, the device comprising:

a first store storing bits representative of transition functions of a state machine model of said finite state machine;

a second store storing bits representative of an estimate of transition functions of said reverse model; and

a processing system comprising

a logical device for transforming said transition functions of the state machine model of said finite state machine into constraints on said reverse model, wherein the reverse model is a reverse model of the state machine model; and

a parameterization processor for applying a parameterization of said constraints to said estimate of transition functions of said reverse model to form transition functions of said reverse model.

10. A device as claimed in claim **9** wherein said estimate of transition functions of said reverse model comprises previous state variables of said finite state machine.

11. The device as claimed in claim **9** wherein said finite state machine includes a logic circuits.

IN THE WRITTEN DESCRIPTION OF THE SPECIFICATION

Applicant presents a replacement paragraph below indicating the changes with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing. All references below to line numbers only include lines on which text is present.

Please rewrite the sentence beginning on page 8, line 4 to read as follows:

A processor 400 further includes a forming device 440 which receives the state variables of the real/reverse models from the third store 300 and also receives the transition functions of the reverse machine from the fourth store 500 and acts to substitute the state variables of the reverse machine with the transition functions of the reverse machine to provide a new set of states which represent the pre-image of the reverse system thus the post-image of the ~~second~~ real system.

PTO/SB/44 (04-04)
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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.	:	6,816,821
DATED	:	November 9, 2004
INVENTOR(S)	:	Geoff Barret

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In col. 5, line 39 should read:

-- of the reverse system thus the post-image of the real --

MAILING ADDRESS OF SENDER

PATENT NO. 6,816,821

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